

A delay-locked loop with precision controlled delay.

#### TECHNICAL FIELD OF THE INVENTION

- 5 The present invention relates to a Delay-Locked Loop (DLL) circuit, comprising input means for a signal that is to be delayed, said input means comprising means for splitting said input signal into a first and a second branch, where the signal in the first branch is connected to a component for delaying the signal, and the signal in the second branch is used as a  
10 reference for the delay caused by the delay component in the first branch

#### STATE OF THE ART

- Time delay circuits are important building blocks in many electronic systems, such as oscillators, measurement instruments, frequency multipliers, wave-  
15 form generators and data and clock recovery circuitry. Most commonly, the desired delay is achieved by use of transmission lines, active circuits, cables (optical or electrical), surface acoustic wave (SAW) circuitry, or magnetostatic wave (MSW) circuitry.

- 20 It is often desired, and indeed sometimes required, that the delay can be varied by a control signal. Commonly, there is a desire for the delay to be a certain fraction of a period, or an integer multiple of such a fraction. In such cases, a Delay-Locked-Loop (DLL) is often used. Usually, a DLL is designed by means of active circuits, most commonly inverters. However, in such  
25 DLL:s, a fixed number,  $N$ , of delay cells is used, which means that only phase delays of  $M/N \cdot 360^\circ$ , where  $0 < M < N$ , can be obtained.

#### SUMMARY OF THE INVENTION

- Accordingly, as described above, there is a need for a DLL-type circuit where  
30 the delay can be chosen by means of a control signal, and where the delay can be chosen in a continuous range, preferably in the entire range of 0-360 degrees.

This need is addressed by the present invention in that it discloses a delay-locked loop circuit with input means for a signal that is to be delayed, the input means comprising means for splitting said input signal into a first and a second branch.

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The signal in the first branch is connected to a component for delaying the signal, and the signal in the second branch is used as a non-delayed reference for the delay caused by the delay component in the first branch. According to the invention, the delay component is a passive tunable delay line, with the circuit comprising tuning means for the tunable delay line.

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The tuning means are affected by said reference signal, and the first branch comprises output means for outputting a delayed signal with a chosen phase delay.

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Suitably, the delay component of the circuit is continuously tunable, and preferably passive, such as a tunable ferroelectric delay line. As alternatives to the tunable ferroelectric delay line, mention can be made of SAW-circuits or MSW-circuits.

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#### BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described in more detail in the following, with reference to the appended drawings, where

Fig 1 shows a schematic block diagram of a known delay-locked loop, and

25 Fig 2 schematically shows the principle behind a delay-locked loop according to the invention, and

Fig 3 shows a more detailed drawing of a delay component of the invention.

#### EMBODIMENTS

30 In order to facilitate the understanding of the present invention, a known kind of delay-locked loop (DLL) circuit 100 is shown in Fig 1. The circuit 100 in fig

1 comprises first input means 110 for an input signal,  $V_{in}$ , which input means split the input signal into a first and a second input branch.

5 The signal in the first input branch of the DLL-circuit is input to a tunable delay component 120, which component thus also has an input possibility for the input of a control or tuning signal, said control signal controlling the delay to which the input signal  $V_{in}$  is exposed.

10 The output from the delay component 120 is split into a first and a second output branch, where the first output branch is used as an output signal from the DLL-circuit, the signal having the desired delay.

The signal in the second output branch from the delay component 120 is used as one of two input signals to a phase detector 150.

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The signal in the second input branch of the DLL is used as the other of the two input signals to the phase detector 150. Thus, the phase detector serves to detect the phase difference or delay between the non-delayed signal and the output signal from the delay component. The output signal from the phase detector corresponds to the phase difference, and is used as the control signal for the delay component 120 in the first input branch of the DLL-circuit. Suitably, the output signal from the phase detector is passed through a low-pass filter 140 before being input to the delay component 120.

25 The DLL of fig 1 can thus provide a phase delay of an input signal, with the phase delay being varied by means of a control signal. However, in contemporary such DLL:s, the most commonly used building block in the delay component are active circuits, usually inverters. The use of, for example, inverters in the DLL will limit the available delays to a certain number of discrete steps.

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In fig 2, a DLL 200 according to the invention is shown, which overcomes this problem of known DLL:s.

The DLL 200 of the invention, in similarity to earlier known DLL:s, comprises  
5 an input means 210 for a signal  $V_{in}$  which is to be delayed. The input means 210 split the input signal into a first and a second branch, and the signal in the first branch is connected to a component 220 for delaying the signal.

As opposed to the conventional DLL 100 shown in fig 1, the DLL 200 of the  
10 invention makes use of a passive tunable delay line 220 as the delaying component. The detailed function and design of this building block 220 of the DLL 200 will be elaborated upon in more detail below, in connection with fig 3.

15 However, one important characteristic of the tunable delay line 220 is that it is possible to tune the delay line so that the electrical distance to be covered by a signal in the line always remains the same, regardless of the frequency of the signal. This means that the phase of a signal entering the delay line 220 will always be the same at a fixed point in the delay line, regardless of  
20 the frequency or wavelength of the signal.

With renewed reference to fig 2, four points with known signal phase have been marked in the delay line 220. The phase at each of these points is known, either by measurement or calculation, and is, by way of example,  
25 shown as  $90^\circ$ ,  $180^\circ$ ,  $270^\circ$  and  $360^\circ$ . As mentioned earlier, the phase at these points will always remain essentially the same, regardless of the wavelength of the input signal, if the delay line is kept properly tuned, which will be explained below.

30 The input signal in the second branch is used as a non-delayed reference for the delay caused by the tuning line in the first branch, which is achieved by means of the input signal in the second branch being connected to a means

250 for phase comparison, in the example shown a phase detector 250. In order to get a second input signal, the phase detector 250 is connected to a point in the delay line with a well defined phase shift, in the example shown 360°.

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Thus, the two input signals to the phase detector are the non-delayed signal from the first branch, and the signal from the second branch which has been shifted 360°. The phase difference between these two signals should accordingly be zero, resulting in an output signal from the phase detector which corresponds to zero phase difference. The output signal from the phase detector 250 is used as a reference signal or control signal for controlling the tunable delay line 220, preferably after having been passed through a low pass filter 240.

15 The filtered output signal from the phase detector 250 is then used as input to a control means 230 for controlling the electrical distance which a signal passing through the delay line will have to cover. In this way, the electrical distance can be kept at a constant and desired value, regardless of the wavelength of the input signal  $V_{in}$ .

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It should be emphasized again that the phase delays shown in fig 2 and mentioned above are only examples, any phase difference can be obtained from the DLL 200 by accessing the proper points in the delay line.

25 As for the function of the filter 240, it could be mentioned that its function is an integrating one.

In addition, the phase detector 250 could in an alternative embodiment compare with another phase position than 360 degrees.

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In fig 3, a tunable delay line 220 as used in fig 2 is shown in more detail: as mentioned previously, the delay line 220 is preferably a tunable ferroelectric

delay line. Such a delay line can consist of the components shown in fig 3: an electrical conductor 305 is supported by a dielectric material 310 which is a ferroelectric material. The ferroelectric material in turn rests on a ground plane 315. The control signal to the control means 230 shown in fig 2 is  
5 connected so that it applies a voltage,  $V_{TUNE}$  between the conductor 305 and the ground plane 315, thereby altering the dielectric constant  $\epsilon$  of the material 310, which causes the electrical distance to be covered by a wave through the component 220 to vary as desired.

10 Suitably, the control signal,  $V_{TUNE}$ , is applied to the conductor via an electrical component such as a resistor or an inductance. This is in order to provide high impedance for the signal, but to simultaneously let through a DC or low frequency bias voltage.

15 Some advantages of the invention that *might* be mentioned are the following:

- Since the circuit of the invention is passive, it doesn't interfere with the input signal, thus offering the possibility of using a modulated input signal.
- 20 • As a passive circuit, it doesn't consume power.
- The circuit of the invention offers a wide tuning range.
- The phase delay offered by the circuit of the invention can be chosen more or less arbitrarily, and changed over a continuous range.